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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/034,834	12/27/2001	Brett W. Murdock	1280.SC11318TH	9616

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TOLER & LARSON & ABEL, L.L.P.
5000 PLAZA ON THE LAKE SUITE 265
AUSTIN, TX 78746

EXAMINER	
INOA, MIDYS	

ART UNIT	PAPER NUMBER
2188	

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9

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/034,834	Applicant(s) MURDOCK ET AL.	
	Examiner Midys Inoa	Art Unit 2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-21* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 17 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. When read in context, it is not clear what the function of a "multiplexor having a control input coupled to the output of the first register, a first data input coupled to the address control pin, a second data input coupled to the first data lane enable, and an output coupled to the output pin" is. The purpose of such multiplexor is not understood since it seems that the system would operate effectively without it.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-5, 8-10, 16, 18-19, 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Chang (2003/0005247 A1).

Regarding Claims 1, 10, 19, and 21, Chang teaches a memory access system in which a first mode of operation, utilizing a first output (Figure 3, Software Interrupt from 100) to provide a first data lane enable (SMI Signal) for facilitating access of a portion of a first memory storage location associated with a first memory address within memory 140; and when in a second mode of operation, utilizing the first output for facilitating designation of a second memory storage location within memory 140. Since the two memory modes of Chang denote different address thresholds to be accessed, the first and second modes facilitate access to different memory storage locations and thus provide different address portions (See Figure 3, Claim 1, and paragraph 0033).

Regarding Claim 16, Chang discloses a memory access system comprising a first register within Real Mode 100 having an output (software interrupt request) to indicate one of a first mode of operation and a second mode of operation; an address control portion 160 having an input coupled to the output of the first register within Real Mode 100, and an output (SMI Signal) to indicate a value of an address bit when in the first mode of operation or when in the second mode of operation; and an output pin coupled to the output of the address control portion 160 and the output of the first data lane enable control portion 180 (see Figure 3).

Regarding Claims 2-4, when accessing a memory it is possible to access memories of different widths. Since Chang teaches the accessing of "addressing ranges" which are being accessed independent in different accessing modes, it is understood that the system could be modified so that these addressing ranges could be represented by independent memories, which

could be byte wide or word wide. Additionally, since a word is always bigger than a byte (which is 8 bits) it is understood that a word wide memory has more than 8 bits associated with it.

Regarding Claim 5, Chang discloses the first output being the first output of a first device 100; and the first and second modes of operation utilize the first output to access a second device 140 external to the first device.

Regarding Claims 8-9, 18, Chang teaches determining the mode of operation when the system realizes which address range needs to be accessed. If the system discovers that the first address range needs to be accessed, it determines that the first mode of operation needs to be in place. The same goes for the scenario when the second address range needs to be accessed. Additionally, the operation which requests the access to one address over another essentially performs as a chip select for the addressing range to be accessed ("a specific chip select", see Page 4, claim 1).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6, 11-15 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (2003/0005247 A1).

Regarding Claim 6, Chang teaches a memory access system in which a first mode of operation is used to access a first addressing range and a second mode of operation is used to

access a second addressing range (Claim 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate into Chang's system the use of a third mode of operation in order to track accesses in a third addressing range which could be that of addresses belonging to an internal storage device. Doing so, would allow the system to more accurately monitor all available storage.

Regarding Claim 11, Chang teaches a memory access system in which a first mode of operation is used to access a first addressing range ("...bits of first address and lane enable...") and a second mode of operation is used to access a second addressing range ("...bits of second address and two lane enables..."). It is understood that "data lane" enable information is simply any signal that can be used to indicate what portion of data is to be accessed. Therefore, any signal being used by the system of Chang to access the various addressing ranges can in fact be a data lane signal (See page 4, claim 1); in addition, it is understood that memory address bits are used in the facilitation of access to a particular memory location. Chang does not teach a third mode of operation in which four lane enables are provided and therefore, a third addressing range can be accessed. It would have been obvious to one of ordinary skill in the art at the time the invention was made to extend the system on Chang to include a third mode of operation in order to allow for the access of a third addressing range. This expanded capability would make the system more versatile as it can manage a greater number of memory areas, thus increasing its capacity.

Regarding Claims 12 and 13, when accessing a memory, it is possible for a system to access memories in locations remote and near, as long as access paths are present. Since Chang teaches the accessing of "addressing ranges" which are being accessed independent in different

accessing modes, it is understood that the system could be modified so that these addressing ranges could be represented by independent memories, which could be of the internal type within the main system, or of the external type outside of the main system.

Regarding Claim 14, Chang teaches determining the mode of operation when the system realizes which address range needs to be accessed. If the system discovers that the first address range needs to be accessed, it determines that the first mode of operation needs to be in place. The same goes for the scenario when the second address range needs to be accessed. Additionally, the operation which requests the access to one address over another essentially performs as a chip select for the addressing range to be accessed ("a specific chip select", see Page 4, claim 1).

Regarding Claim 15, Chang teaches a memory access system in which a first mode of operation is used to access a first addressing range and a second mode of operation is used to access a second addressing range (Claim 1). Since the two memory modes of Chang denote different address thresholds to be accessed, it is known that the first and second modes facilitate access to different memory storage locations and thus provide different address portions (See Figure 3, Claim 1, and paragraph 0033). It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate into Chang's system the use of a third mode of operation in order to track accesses in a third addressing range which could be that of addresses belonging to an internal storage device. Since the different addressing modes of operation provide access to different addressing thresholds, these have to be represented by providing different address portions. If three modes of operation are provided in the system, the

three different addressing thresholds could be accessed through three different address bit locations (A(1), A(0), and A(n+1)).

Regarding Claim 20, Chang teaches the invention as set forth by claim 19 above. Chang does not teach the use of a third mode of operation to access a third memory device, which is internal to the system. It would have been obvious to one of ordinary skill in the art at the time the invention was made to extend the system on Chang to include a third mode of operation in order to allow for the access of a third addressing range. This expanded capability would make the system more versatile as it can manage a greater number of memory areas, thus increasing its capacity. Additionally, it is possible for an access system to access memories in locations remote and near, as long as access paths are present. Since Chang teaches the accessing of "addressing ranges" which are being accessed independent in different accessing modes, it is understood that the system could be modified so that these addressing ranges could be represented by independent memories, which could be of the internal type within the main system, or of the external type outside of the main system.

Allowable Subject Matter

6. Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The Prior Art of Record does not teach an address bit used to extend an address range when a memory having a width less than a word is being accessed.

Response to Arguments

7. Applicant's arguments filed on January 18th, 2004 have been fully considered but they are not persuasive.

Regarding the arguments for Claims 1, 10, 19, and 21, Chang teaches a memory access system in which a first mode of operation, **utilizing a Software Interrupt request as an output** to provide a first data lane enable (**SMI Signal**) for facilitating access of a portion of a first memory storage location associated with a first memory address within memory 140; and when in a second mode of operation, utilizing the **Software Interrupt request as an output** for facilitating designation of a second memory storage location within memory 140. Since the two memory modes of Chang denote different address thresholds to be accessed, **the first and second modes facilitate access to different memory storage locations and thus provide different address portions** (See Figure 3, Claim 1, and paragraph 0033).

Regarding the arguments for Claim 16, Chang discloses a memory access system comprising a **first register within Real Mode 100** having an output (software interrupt request) to indicate one of a first mode of operation and a second mode of operation; an **address control portion 160** having an input coupled to the output of the first register within Real Mode 100, and an output (**SMI Signal**) to indicate a value of an address bit when in the first mode of operation or when in the second mode of operation; and an output pin coupled to the output of the address **control portion 160** and the output of the first data lane enable control portion 180 (see Figure 3).

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Inoa whose telephone number is (703) 305-7850. The examiner can normally be reached on M-F 7:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Midys Inoa
Examiner
Art Unit 2188

MI

JACK A. LANE
PRIMARY EXAMINER